In the Claims:

1. (Currently Amended) A method for ~~increasing the size of a portion of main trench structures of a semiconductor component, said portion of each main~~ manufacturing an integrated circuit comprising a trench structure having sidewalls ~~and is to be~~ formed in a depth under the surface of a semiconductor substrate, said method comprising:

providing said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching;

~~arranging~~ defining at the surface of the semiconductor substrate first areas of a rectangular surface ~~grid,~~ grid having an x axes and a y axes; ~~said first areas being provided in checkered fashion for forming said main trench structures and alternating with second areas of said rectangular surface grid, said second areas being provided for forming secondary structures in a section of the semiconductor substrate that is near said surface thereof;~~

~~setting x, y~~ positioning said x and y axes of the surface grid to be parallel to the crystal faces that are less resistant to etching; and

etching a surface opening of said trench structures in said first areas, and etching said sidewalls of said portion of the ~~formed main~~ trench structures formed in a depth under said surface of said semiconductor substrate by etching said crystal faces that are less resistant to etching so as to expand said sidewalls [[to]] beneath said second areas of said surface grid.

2. (Currently Amended) The method of claim 21, wherein said surface opening of a ~~large~~ trench structure opening is imaged onto the first areas of the surface of the semiconductor

substrate by means of an exposure ~~device with the x, y axes of the surface grid parallel to the crystal faces of the semiconductor substrate that are less resistant to etching.~~ device.

3. (Currently Amended) The method of claim 2, wherein prior to imaging, a mask opening defining rectangular sides ~~having rectangular mask openings~~ in a layout of the ~~large~~ trench structure is oriented ~~in accordance~~ so that the rectangular sides are parallel with the crystal faces of the semiconductor substrate that are less resistant to etching.

4. (Previously Presented) The method of claim 21, wherein a semiconductor wafer is provided as the semiconductor substrate and a marking identifying a crystal orientation of the crystal lattice is provided at the semiconductor wafer.

5. (Original) The method of claim 4, wherein a crystal orientation identifying the orientation of the crystal faces that are less resistant to etching is identified by the marking.

6. (Original) The method of claim 5, wherein the marking is used for the orientation of a mask in an exposure device.

7. (Currently Amended) The method of claim 21, further comprising ~~providing~~ etching the [[main]] trench ~~structures~~ structure opening at the surface of the semiconductor substrate with an oval cross section.

8. (Previously Presented) The method of claim 21, wherein monocrystalline silicon is provided as the material of the semiconductor substrate.

9. (Original) The method of claim 8, wherein the surface grid is oriented in accordance with a <100> crystal orientation of the monocrystalline silicon.

10. (Previously Presented) The method of claim 9, wherein during the etching process, the <100> crystal faces having a lower etching resistance are etched more rapidly than the <110> crystal faces that are more resistant to etching.

11. (Currently Amended) The method of claim 21, wherein upper sections of the [[main]] trench structures, between the surface of the semiconductor substrate and at least one lower edge of the secondary structures, are provided with a protective layer that is resistant to the etching process that ~~expanding~~ expands said sidewalls of said [[main]] trench structure.

12. (Currently Amended) The method of claim 21, wherein the [[main]] trench structures are functionally designed as storage capacitances.

13. (Previously Presented) The method of claim 21, wherein the secondary structures are selection transistors formed in the second areas for use with the storage capacitances of DRAM cells.

14-20. (Canceled)

21. (Currently Amended) A method for increasing a structure size of [[main]] trench structures in a depth under a surface of a semiconductor substrate, said method comprising:

providing said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less

resistant to etching;

~~arranging~~ defining first areas for forming said [[main]] trench structures in a ~~checkered~~ checker-board fashion in a rectangular surface ~~grid,~~ grid having an x axes and a y axes, at a surface of the semiconductor substrate, said first areas ~~respectively~~ alternating with second areas for ~~respectively alternating with a second areas for respectively~~ forming secondary structures ~~substantially~~ in a section of the semiconductor substrate that is near a surface thereof;

~~setting x, y~~ positing said x axes and said y axes of the surface grid to be parallel to the crystal faces that are less resistant to etching; and

performing area-selective etching to increase the structure size of the [[main]] trench structures in said depth under said semiconductor substrate's ~~surface~~ surface, ~~so that the~~ said structure size of said ~~increased main~~ trench structures [[are]] expanded [[to]] along said crystal faces that are less resistant to etching beneath ~~sections of~~ said second areas for forming said secondary ~~structures.~~ structures by said area selective etching.

22. (Currently Amended) The method of claim 1, wherein a ~~large structure having the main~~ trench ~~structures~~ structure is imaged onto the surface of the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces of the semiconductor substrate that are less resistant to etching.

23. (Currently Amended) The method of claim 22, wherein prior to said imaging, a mask having rectangular mask openings in a layout of the large structure is oriented ~~in accordance~~ such that the sides of the rectangular mask opening are parallel with the crystal faces of the semiconductor substrate that are less resistant to etching.

24. (Previously Presented) The method of claim 1, wherein a semiconductor wafer is provided as the semiconductor substrate and a marking identifying a crystal orientation of the crystal lattice is provided at the semiconductor wafer.

25. (Previously Presented) The method of claim 24, wherein said crystal orientation represents the orientation of the crystal faces that are less resistant to etching is identified by the marking.

26. (Previously Presented) The method of claim 25, wherein said marking is used for orienting a patterned mask.

27. (Currently Amended) The method of claim 1, further comprising ~~providing~~ etching the [[main]] trench ~~structures~~ structure opening at the surface of the semiconductor substrate with an oval cross section.

28. (New) A method for manufacturing an integrated circuit comprising a trench structure having sidewalls formed in a depth under the surface of a semiconductor substrate, said method comprising:

providing said semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching;

defining at the surface of the semiconductor substrate first areas of a rectangular surface grid having an x axes and a y axes, said first areas being located in checker-board fashion for forming said trench structures, said first areas alternating with second areas of said rectangular

surface grid, said second areas being provided for forming secondary structures in a section of the semiconductor substrate that is near said surface thereof;

positioning said x and y axes of the surface grid to be parallel to the crystal faces that are less resistant to etching; and

etching a surface opening of said trench structures in said first areas.

29. (New) The method of claim 28, wherein the secondary structures are selection transistors.

30. (New) The method of claim 28, wherein a trench structure is imaged onto the surface of the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces of the semiconductor substrate that are less resistant to etching.

31. (New) The method of claim 30, wherein prior to said imaging, a mask having rectangular mask openings in a layout is oriented such that the sides of the rectangular mask opening are parallel with the crystal faces of the semiconductor substrate that are less resistant to etching.

32. (New) The method of claim 28, wherein a semiconductor wafer is provided as the semiconductor substrate and a marking identifying a crystal orientation of the crystal lattice is provided at the semiconductor wafer.

33. (New) The method of claim 32, wherein said crystal orientation represents the orientation of the crystal faces that are less resistant to etching is identified by the marking.

34. (New) The method of claim 33, wherein said marking is used for orienting a patterned mask.

35. (New) The method of claim 28, further comprising etching the trench structure opening at the surface of the semiconductor substrate with an oval cross section.